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-- Company:

-- Engineer:

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-- Create Date: 17:35:37 02/05/2014

-- Design Name:

-- Module Name: cnt - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

**use** IEEE**.**NUMERIC\_STD**.ALL;**

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

**ENTITY** cnt\_gen **IS**

**GENERIC** **(**width **:** NATURAL **:=** 4**;**

modulo **:** NATURAL **:=** 10**);**

**PORT** **(**ck**,** c\_in **:** **IN** STD\_LOGIC**;**

q **:** **BUFFER** UNSIGNED **((**width**-**1**)** **downto** 0**);**

SW7**:** **in** STD\_LOGIC**;**

Ax**:** **IN** UNSIGNED **(**3 **downto** 0**);**

c\_out **:** **BUFFER** STD\_LOGIC**);**

**END** cnt\_gen**;**

**ARCHITECTURE** behav **OF** cnt\_gen **IS**

**BEGIN**

**PROCESS**

**BEGIN**

**IF** SW7 **=** '0' **THEN**

q **<=** Ax**;**

**END** **IF;**

**WAIT** **UNTIL** **RISING\_EDGE(**ck**);**

**IF** c\_out **=** '1' AND SW7 **=** '1' **THEN**

q **<=** **TO\_UNSIGNED((**modulo**-**1**),**4**);**

**ELSIF** c\_in **=** '1' AND SW7 **=** '1' **THEN**

q **<=** q **-** 1**;**

**END** **IF;**

**END** **PROCESS;**

c\_out **<=** '1' **WHEN** **(**c\_in **=** '1'**)** AND **(**q **=** "0000"**)** **ELSE** '0'**;**

**END** behav**;**